IN THE SPECIFICATION:

Please REPLACE the paragraph beginning at page 1, line 6, with the following paragraph:

The present invention relates to a microcontroller that has a debug support unit (hereinafter referred to as a DSU), and more particularly to a microcontroller that has a DSU, which is capable of performing an instruction fetch operation and data access at high-speed with respect to an in-circuit emulator (ICE) which stores a program ~~s~~ and data for debugging and whose function is to monitor the state of the CPU at the time of execution of program instruction code.

Please REPLACE the paragraph beginning at page 3, line 1, with the following paragraph:

However, the external ICE, in addition to storing programs and data, or the like, has the function of monitoring the internal state of the microcontroller. A great number of signal lines are employed to monitor this internal state, therefore such a large number of signal lines occupy the majority of the external pins of the microcontroller. As a result, the number of external pins that can be utilized with the tool bus for the transfer of data and addresses, and the like, between the DSU and ICE is limited, and this tool bus cannot ~~have~~ implement a large number of multiple-bit structures like the data bus inside the microcontroller, which may utilize a greater number of bits. Consequently, addresses and data must be transferred by serial transfer, and by using time-sharing, via a tool bus, which is between the DSU and ICE, that has a structure of a low number of bits.

Please REPLACE the paragraph beginning at page 14, line 5, with the following paragraph:

Fig. 3 is a figure that illustrates further principles of the present embodiment. As shown in the example of the constitution of the access control unit of Fig. 3A, this access control unit has a status-information generation circuit 20, a status output circuit 22, a parallel to serial conversion circuit 24, a data-output circuit 28, and, in addition, an instruction address selection circuit 30. In this example, at a point in time when status information generation circuit 20 output a status information signal S20 in response to an instruction fetch request signal 6 from the CPU and an instruction-fetch operation is complete, in other words, at a point in time when, after data-output circuit 28 has performed the serial transfer of an instruction address to tool bus 16 or output a branchless signal, the instruction code has been received, if this status information generation circuit 20 has not yet received an instruction-fetch signal from the CPU, only at a time

when there is space in the receive buffer of tool bus 16 (not shown), the status information generation circuit 20 outputs a new status information signal S20 for an instruction prefetch operation. Status information signal S20 for this instruction prefetch operation contains branchless information, and in response thereto, the instruction address selection circuit 30 outputs the next instruction address, which is obtained by incrementing the instruction address from the CPU by two, in place of the instruction address from the CPU. Consequently, following parallel to serial conversion of the instruction address of the next address, the converted address is output from data-output circuit 28 to tool bus 16. In the above example, an instruction address containing a ~~branch-less~~branchless signal is incremented in steps of two.

Please REPLACE the paragraph beginning at page 15, line 7, with the following paragraph:

In other words, even if a subsequent instruction fetch request signal has not been received from the CPU, since the tool bus is in an unusable state when the current instruction-fetch operation is complete, as long as there is space in the receive buffer, the status information generation circuit 20 commence an instruction prefetch operation. Consequently, it becomes possible to efficiently employ tool bus 16, whose bit number is small, and, thereafter, at a time when the subsequent instruction fetch request signal has arrived from the CPU, instruction data can be sent in response within a shorter cycle or immediately.